IN THE CLAIMS

1. (Currently amended) A bonding pad structure of a semiconductor device, said bonding pad structure comprising:

a substructure formed on a semiconductor substrate;

a first dielectric layer formed on the substructure;

a polysilicon film plate formed on the first dielectric layer;

a second dielectric layer formed overlying the polysilicon film plate, the second dielectric layer having a first opening that expose a region of the polysilicon film plate,

a first metal layer formed on the polysilicon film plate through the first opening;

an inter-metal dielectric (IMD) layer formed overlying the first metal layer, the inter-metal dielectric layer having a second opening that exposes a region of the first metal layer;

a second metal layer formed on the first metal layer in the second opening; and

a passivation layer formed overlying the second metal layer, the passivation layer having a third opening that exposes a region of the second metal layer as a bonding pad, the bonding pad ~~directly overlying~~ positioned above and overlapping the polysilicon film plate.

2. (Previously presented) A bonding pad structure according to claim 1, wherein the first metal layer is formed having a somewhat horseshoe-shaped cross-section.

3. (Previously presented) A bonding pad structure according to claim 2, wherein a region of the second metal layer is disposed within a recessed area of the first metal layer.

4. (Previously presented) A bonding pad structure according to claim 1, wherein the second metal layer has a somewhat horseshoe-shaped cross-section.

5. (Previously presented) A bonding pad structure according to claim 1, wherein the substructure comprises circuitry configured to provide a dynamic random access memory.

6. (Previously presented) A bonding pad structure according to claim 1, wherein the first dielectric layer is a boron phosphor silicate glass (BPSG) layer.

7. (Previously presented) A bonding pad structure according to claim 1, wherein the first dielectric layer has a thickness of between about 3000-4000 Å.

8. (Previously presented) A bonding pad structure according to claim 1, wherein the polysilicon film plate has a thickness of about 1000-2000 Å.

9. (Previously presented) A bonding pad structure according to claim 1, wherein the first and second metal layers are formed of aluminum.

10. (Previously presented) A bonding pad structure according to claim 1, wherein the first metal layer has a thickness of approximately 7000-7500 Å.

11. (Previously presented) A bonding pad structure according to claim 1, wherein the second metal layer has a thickness of about 8500-9000 Å.

12. (Previously presented) A bonding pad structure according to claim 1, wherein the wire bonding is beam lead bonding.

13. (Previously presented) A semiconductor package comprising a semiconductor chip having the bonding pad structure of claim 1.

14. (Previously presented) A semiconductor package module having a semiconductor chip mounted thereon, wherein the semiconductor chip comprises a bonding pad structure according to claim 1.

15. (Withdrawn) A method of fabricating a bonding pad of a semiconductor device, said method comprising:

forming a polysilicon film plate on a semiconductor substrate having a substructure formed thereon to improve the ability of the bonding pad to withstand stress during wire bonding;

forming a second dielectric layer on the semiconductor substrate over the polysilicon film plate;

etching a region of the second dielectric layer to expose a region of the polysilicon film plate;

forming a first metal layer over an area of the second dielectric layer, wherein said first metal layer is configured to contact the polysilicon film plate through the etched region of the second dielectric layer;

forming an inter-metal dielectric (IMD) layer on the semiconductor substrate over the first metal layer and the second dielectric layer;

etching a region of the IMD layer in which a bonding pad will be formed;

forming a second metal layer over an area of the IMD layer, wherein said second metal layer is configured to contact the first metal layer through the etched region of the IMD layer;

forming a passivation layer over the second metal layer; and

etching a region of the passivation layer to expose a bonding pad area.

16. (Withdrawn) A method according to claim 15, further comprising forming a first dielectric layer on the substructure before the forming the polysilicon film plate.

17. (Withdrawn) A method according to claim 15, wherein the polysilicon film plate has a thickness of about 1000-2000 Å.

18. (Withdrawn) A method according to claim 15, wherein forming the passivation layer comprises:

forming an oxide layer by high density plasma deposition; and

forming a nitride layer on the oxide layer by PECVD.

19. (Withdrawn) A method according to claim 15, wherein a portion of the second metal layer is disposed within a recessed portion of the first metal layer.

20. (Currently amended) A bonding pad structure of a semiconductor device, said bonding pad structure comprising:

a substructure formed on a semiconductor substrate;

a first dielectric layer formed on the substructure;

a polysilicon film plate formed on the first dielectric layer and configured to improve the resistance of the bonding pad to stress created during wire bonding;

a first metal layer formed on the polysilicon film plate, wherein the first metal layer is formed having a recessed area;

a second metal layer formed on the first metal layer, wherein a portion of the second metal layer is arranged within the recessed area of the first metal layer to improve the resistance of the bonding pad to stress; and

a passivation layer formed overlying the second metal layer having an opening that exposes a region of the second metal layer as a bonding pad, the exposed region of the second metal layer ~~directly overlying~~ positioned above and overlapping the polysilicon film plate.

Cancel claim 21, without prejudice.

22. (Previously presented) The bonding pad structure according to claim 20, wherein the polysilicon film plate absorbs thermo-mechanical stress induced in the bonding pad during wire bonding.

23. (New) A bonding pad structure of a semiconductor device, said bonding pad structure comprising:

a substructure formed on a semiconductor substrate;

a first dielectric layer formed on the substructure;

a polysilicon film plate formed on the first dielectric layer;

a second dielectric layer formed overlying the polysilicon film plate, the second dielectric layer having a first opening that expose a region of the polysilicon film plate,

a first metal layer formed directly on the polysilicon film plate through the first opening;

an inter-metal dielectric (IMD) layer formed overlying the first metal layer, the inter-metal dielectric layer having a second opening that exposes a region of the first metal layer;

a second metal layer formed directly on the first metal layer in the second opening; and

a passivation layer formed overlying the second metal layer, the passivation layer having a third opening that exposes a region of the second metal layer as a bonding pad, the bonding pad overlying the polysilicon film plate.